EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"7236921".pn.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S2	77	("20020052729"|"20020116168"|"20020156885"|"20020156998"|"20030056071"|"20030149961"|"4176258"|"4757534"|"5127103"|"5202687"|"5321828"|"5325512"|"5331571"|"5371878"|"5493723"|"5546562"|"5559996"|"5572665"|"5574892"|"5587957"|"5590354"|"5630052"|"5630102"|"5663900"|"5691898"|"5748875"|"5752013"|"5802290"|"5805792"|"5889988"|"5911059"|"5964893"|"5978584"|"5999725"|"0559996"|"6009270"|"6016554"|"6016563"|"6034538"|"6058263"|"6075941"|"6094730"|"6107826"|"6144327"|"6161199"|"6173419"|"6185522"|"6202044"|"6223144"|"6223272"|"6289300"|"6298320"|"6302268"|"6347395"|"6356862"|"6366878"|"6374370"|"6385742"|"6460172"|"6466898"|"6487700"|"6516428"|"6564179"|"6581191"|"6618854"|"6718294"|"6810442"|"6816544"|"6829727"|"6922821"|"6957180"|"6967960"|"7076420"|"7089175"|"7099818"|"7162410"|"7236921").PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S3	7	S2 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 09:25
S4	6	S3 and clock$1	US-PGPUB; USPAT	OR	ON	2008/01/22 09:44
S5	13	("20020052729"|"20020156998"|"20030056071"|"20030149961"|"4176258"|"4757534"|"5691898"|"5802290"|"6016563"|"6034538"|"6460172"|"6816544"|"6967960").PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:50
S6	1	"4757534".PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 09:51
S7	1	"5357626".PN.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:06
S8	36	703/23,26.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15
S9	0	716/224.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15
S10	9	714/28.ccls. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:15

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S11	59	cypress adj semiconductor$.as. and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S12	0	S11 and (sleep and (stall or halt))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:16
S13	3	S11 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S14	1	S11 and stall	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S15	1549	cypress adj semiconductor$.as.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:17
S16	15	S15 and sleep.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S17	10	S16 and clock$1.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S18	18	S15 and (sleep.clm. or stall.clm.)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:18
S19	10	S18 and clock$1.clm.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:21
S20	16	nemecek-craig$.in.	US-PGPUB; USPAT	OR	ON	2008/01/22 10:27
S21	691	((device adj under adj test) or dut) and @pd>"20070829"	US-PGPUB; USPAT	OR	ON	2008/01/22 10:27
S22	0	S21 and (sleep near (mode or function or operation))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:29
S23	0	S21 and (stall near (mode or function or operation))	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S24	0	S21 and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S25	5	S21 and sleep	US-PGPUB; USPAT	OR	ON	2008/01/22 10:28
S26	343	(sleep near (mode or function or operation)) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:30
S27	2	S26 and ((device adj under adj test) or dut)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:30
S28	5	(stall near (mode or function or operation)) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:31
S29	2	S27 and ((device adj under adj test) or dut)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38
S30	0	S28 and emulat$3	US-PGPUB; USPAT	OR	ON	2008/01/22 10:37
S31	55	((device adj under adj test) or dut) and (clock near off)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38
S32	5	S31 and (sleep or stall or halt)	US-PGPUB; USPAT	OR	ON	2008/01/22 10:38

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D Jones, DM Lewis - Custom Integrated Circuits Conference, 1995., Proceedings of ..., 1995 - ieeexplore.ieee.org
... other functional unit is awakened from its **sleep** condition ... In comparison, a Xilinx **FPGA** has 8i7 I/O pads ... interconnect is used in a Xilinx -based **emulator** at some ...
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... is seen in early (pre-silicon) debug (ie hardware **emulation** or in **FPGA** devices) with a ... by a semaphore synchronization until it is put to **sleep** waiting for ...
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... most common type, can be solved by Forwarding or **Stall** ... the pipeline, the worst the branch penalty in **clock** cycles ... Until the trap is taken, turn **off** all writes ...
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... extensive paral- lelism and high **clock** frequencies to ... models to be implemented in a single **FPGA**. ... ignores incorrect path instructions and **stalls** until correct ...
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JR Andrews - 2004 - books.google.com
... code into a suitable bitstream file for programming the **FPGA**. ... the CPU board for in-circuit **emulation** of ARM ... not active) can be minimized using **sleep** modes and ...
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... XScale + **FPGA** ... ARM ISA **emulation** support added to SimpleScalar tool set ... eg, branch mispredictions, cache misses, writeback **stalls** ...
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... groups) operating at a moderate **clock** rate (500MHz). ... instructionbefore it is available, the pipeline will **stall**. ... The **sleep** instruction, the wakeup signal, the ...
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D Bekker - 2007 - ritdml.rit.edu
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... of a device multiplexing the media streams, and the **emulation** of the ... cycles entry in Table 1 represents the number of **clock** cycles without **stalls** due to ...
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... on the StrongARM uses a software **emulation** to implement it ... is also performed to determine **stalls** and a ... However, reverting to **sleep** mode between duty cycles may ...
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... cache and the local memory of the **FPGA** must be ... flow of instructions in CPU pipelines, with reduced **stalls**. ... Therefore, they **sleep** until they are forced into the ...
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... changes, but hold **off** net-drivers-2.5 because of a change that needs. +more discussion. +. ... If both this SCSI **emulation** and native ATAPI support are compiled. ...
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